PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-334459

(43)Date of publication of application : 02.12.1994

(51)Int.Cl. H03G 11/08
H03G 3/20
H03G 5/16

(21)Application number : 05-139493

(22)Date of filing : 18.05.1993

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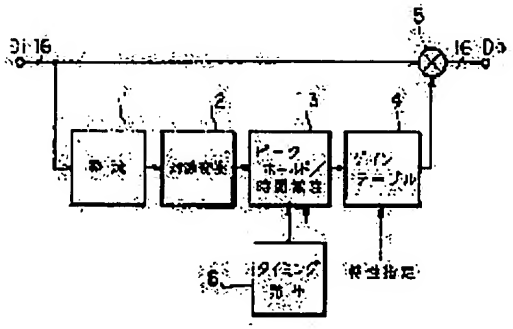
(54) DIGITAL SIGNAL PROCESSOR

(57)Abstract:

PURPOSE: To obtain the digital signal processor coping with a signal of a wide dynamic range with simple circuit configuration without impairing the degree of freedom of the characteristic.



CONSTITUTION: The digital signal processing circuit is made up of a rectifier circuit 1, a logarithmic transformation circuit 2, a peak hold/time attenuation circuit 3, a gain table 4, a multiplier 5 and a timing generating circuit 6. The rectifier circuit 1 obtains an absolute value of input data. The logarithmic transformation circuit 2 transforms linear input data into a logarithmic data. The peak hold/time attenuation circuit 3 applies peak holding and timewise attenuation processing to inputted instantaneous logarithmic data to obtain a rough logarithmic envelope. The gain table 4 has a nonlinear gain characteristic and inputs logarithmic data as an address to provide an output of a gain in response to the input level. The multiplier 5 multiplies the gain by the input data to provide an output of output data processed by the nonlinear characteristic.